REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended each of the previously considered claims to recite that the insulating film on the oxidation prevention film is removed by chemical mechanical polishing, thereby forming a polished surface; and that after the removing, oxidation, or selective oxidation, of the semiconductor substrate having the planarized surface is performed, so as to oxidize a specified portion of the semiconductor substrate, at the upper end portion of the trench. Note, for example, page 7 of Applicants' specification; see also pages 13 and 14 of Applicants' specification.

In addition, Applicants are adding new claims 54 and 55 to the application. Claim 54 recites processing steps (a), (b), (c), (d), (e), (g) and (h) as in previously considered claim 1; and, additionally, recites (1) that the trench is formed by a first trench forming step, using isotropic etching, so as to form a radius of curvature in a proximity of the upper end portion (of the trench), and by a second trench forming step using anisotropic etching, and (2) performing an additional thermal oxidation, after burying the buried insulating film, so as to selectively oxidize the semiconductor substrate at the upper end portion of the trench. Claim 55, dependent on claim 54, recites that the further step of performing an additional thermal oxidation is performed after the removing step (f). Note, for example, the third embodiment as described, for example, on pages 19-25 of Applicants' specification.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the

references applied by the Examiner in rejecting claims in the Office Action mailed March 5, 2003, that is, the teachings of the U.S. patents to Mehta, No. 5,679,599 (Mehta '599) and to Mehta, et al., No. 5,646,063, and Japanese Patent Document No. 01-107554 (Kojiro), under the provisions of 35 USC §102 and 35 USC §103.

It is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such a method of fabricating a semiconductor device as in the present claims, including, inter alia, after burying the buried insulating film in a trench, with the insulating film also formed on an oxidation prevention film, removing the insulating film on the oxidation prevention film by chemical mechanical polishing, thereby forming a polished surface; and, after this removing, performing oxidation (more specifically, selective oxidation) of the semiconductor substrate having the polished surface, so as to oxidize only a portion of the semiconductor substrate, at the upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench, providing a curvature (increased radius of curvature) of the upper end portion of the trench. See claims 1, 2, 4, 5, 9, 10, 15, 41, 43 and 45-47.

In addition, it is respectfully submitted that the teachings of the applied prior art would have neither disclosed nor would have suggested such a method of fabricating a semiconductor device as in the present claims, including wherein a trench is formed having a desired depth, the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate, the trench being formed by a first trench forming step, using isotropic etching, so as to form a radius of curvature in a proximity of the upper end portion of the trench, and by a

second trench forming step using anisotropic etching, the trench portion formed in a semiconductor substrate (exposed in the trench) being oxidized and a buried insulating film being buried into the trench, thus oxidized, this insulating film also being formed on the oxidation prevention film; and after burying the buried insulating film, performing an additional thermal oxidation so as to selectively oxidize the semiconductor substrate at the upper end portion of the trench and removing the insulating film on the oxidation prevention film; and eliminating the oxidation prevention film formed on the semiconductor substrate. See claim 54.

Furthermore, it is respectfully submitted that the applied references would have neither disclosed nor would have suggested such fabrication method as in the present claims, utilizing the two steps for forming the trench, and including the additional thermal oxidation step, after the burying step, with this additional thermal oxidation step being performed after removing the insulating film on the oxidation prevention film. Note claim 55.

In addition, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested the other aspects of the present invention as in the present claims, having the processing steps discussed previously, and also including formation of a shallow trench and then forming trenches having a predetermined depth to the shallow trenches (note, for example, claims 2, 5 and 43); and/or wherein the step of eliminating the oxidation prevention film is performed after selective oxidation of the semiconductor substrate at the upper end portion (note, for example, claims 42, 44 and 48); and/or material, and techniques of formation, of the buried insulating film as in claims 18-38; and/or

wherein an angle between the circuit formation surface of a substrate and a side surface of the semiconductor substrate forming the trench is within a range as in claim 13; and/or wherein the oxidation of the trench portion to provide the upper end portion of the trench with a curvature is a thermal oxidation (see, for example, claim 17).

The invention as presently claimed in the above-identified application is directed to a method of manufacturing a semiconductor substrate, or semiconductor device, having a trench isolation structure. A process forming a so-called "trench isolation structure", which forms trenches extending into the substrate from the substrate surface and then selectively oxidizes the trenches to form a thermal oxide film, has been employed to form insulation/isolation structure of semiconductor devices, as described in the paragraph bridging pages 1 and 2 of Applicants' specification.

In the trench isolation structure, end points (corner points) essentially exist near the trench upper end portion of the semiconductor substrate. Stress concentration fields (both mechanical stress and electrical stress) are formed near these end points. Because such stress concentration fields are formed, the shape of the substrate, particularly near the trench upper end portion, is oxidized in some cases into a pointed shape having an acute angle, as shown by the structure represented by reference character 4 in Fig. 1C of Applicants' disclosure. If such an acute angle portion 4 remains on the semiconductor surface, however, concentration of electric field occurs at this portion during the circuit operation and deteriorates the breakdown voltage characteristics of transistors, capacitors, etc.,

formed utilizing such substrate. Moreover, mechanical stress fields, which are disadvantageous, are also formed. See the paragraph bridging pages 3 and 4 of Applicants' specification.

Against this background, Applicants provide a process wherein trench isolation can be utilized, without causing deterioration of breakdown voltage characteristics of transistors and capacitors utilizing the substrate with the trench isolation structure, while providing semiconductor devices having a high reliability. Moreover, Applicants fabricate such structure utilizing a relatively simple technique.

Applicants have found that the desired structure can be achieved by preventing a substrate shape in the proximity of the upper end portion of the device isolation trench from becoming an acute angle; and, by the present invention, provide simple techniques for preventing such acute angle. Specifically, according to an aspect of the present invention, Applicants provide procedures which can easily and effectively provide a curvature (increased curvature) only of an upper end portion of the trench, by selectively oxidizing only the upper end portion, so as to prevent the aforementioned acute angle. For example, and specifically, according to aspects of the present invention, after burying the buried insulating film, this insulating film also being formed on an oxidation prevention film on the semiconductor substrate, this insulating film on the oxidation prevention film is removed and then the upper end portion of the trench is oxidized while the lower portion of the trench is substantially not oxidized, whereby the semiconductor substrate can be oxidized (selectively) at only the upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the

trench. Removal of the insulating film from the oxidation prevention film, prior to oxidation (selectively), can, for example, uncover upper end portions of the trench, facilitating oxidation of the upper end portions. Moreover, more generally, after burying the buried insulating film and removal of this insulating film from the oxidation prevention film on the substrate, an upper end portion of the trench can be provided with the curvature (increased curvature). This prevention of the acute angle can be achieved, for example, by thermal oxidation of substantially only the upper end portion of the trench; e.g., by forming bird's beaks at the upper end portion of the trench.

As is clear according to the specification of the present application, since the buried insulating film 9 (see, e.g., Fig. 2(g)) has already been formed inside the trench of the silicon substrate 1, especially wherein the insulating film 9 has been removed from on the oxidation prevention film (e.g., at the upper end portion of the trench), oxidation proceeds from near the trench upper end portion 12, and the inside of the trench is hardly oxidized. That is, a longer time is necessary for oxidation seeds to diffuse inside the buried insulating film 9 before reaching the silicon substrate 1 at lower portions of the trench, than when the silicon substrate is directly oxidized. Therefore, oxidation hardly proceeds substantially near the bottom of the trench. On the other hand, a weak boundary layer of the coupling portion deposited by chemical vapor deposition or sputtering to the trench sidewalls and the upper surface of the trench exists at the trench upper end portion 12, and oxidation seeds can diffuse at a relatively high rate along this weak boundary layer, and especially where the insulating film has been removed from on the oxidation

prevention film. As a result, oxidation seeds are supplied to the trench upper end portion 12 within a short time, so that only the portions in the proximity of the trench upper end portion 12 are oxidized preferentially and the formation of the radius of curvature of the trench upper end portion 12 is promoted. Note, for example, the paragraph bridging pages 14 and 15 of Applicants' specification.

According to another aspect of the present invention, the increased curvature is provided by a two-step etching in forming the trench, with a subsequent additional thermal oxidation after filling the trench, so that only upper end portions of the trench are primarily oxidized by the additional thermal oxidation. A first step is performed isotropically, so as to provide a radius of curvature to the upper end portion of the trench, and a second step is performed anisotropically to provide the trench having a desired depth.

It is emphasized that according to the present invention, Applicants have recognized that curvature formation including, for example, at the upper end portion of the trench, is important to reduce concentration of both mechanical and electrical stress fields, in order to provide a reliable device with shallow trench insulation. Having recognized this, Applicants provide simple techniques for increasing curvature (providing roundness) at the top corners of the trench; and, according to various aspects of the present invention, provide such increased curvature by, e.g., additional oxidation after filling the trench and, e.g., after removal of filler material on the oxidation prevention film and prior to removal of the oxidation prevention film, and/or by appropriate etching in forming the trench. Only a small amount of oxidation is utilized to provide the roundness at the upper corners of the trench (for

example, the oxidation is performed for only a short time; and, according to the invention as presently claimed in various aspects, the trench filling material (of, for example, chemical vapor deposited oxide) on the oxidation prevention film is removed therefrom prior to performing the additional oxidation to increase curvature), with the oxidation prevention film being removed after the additional oxidation.

Thus, according to the present invention, simple techniques are provided to achieve increased radius of curvature at top corners of the trench, so as to reduce concentration of both mechanical and electrical stress fields, so as to provide reliable semiconductor devices.

Mehta, et al. discloses a fabrication method for creating wide and narrow isolation regions, while at least reducing dishing problems. The method includes steps of selectively providing an etch resist layer over the wide spacing and exclusive of the narrow spacing, etching the semiconductor structure to increase the depth of the narrow spacing to form a narrow trench, growing an oxide liner in the narrow trench and in the wide spacing, providing a trench fill oxide layer over the nitride layer and the oxide liner in the wide spacing and in the narrow trench, and field oxidizing the wide spacing and the narrow trench. See column 2, lines 4-12. Note also column 2, lines 23-33 and 51-53. Note also column 3, lines 5-7, describing that the processing described in Mehta, et al. eliminates or reduces dishing due to different widths of trench isolation regions.

A specific embodiment is described and shown with respect to Figs. 2-7 of Mehta, et al. Note column 4, line 43 to column 5, line 65, of Mehta, et al. This

process includes, after providing layer 60 to fill, inter alia, a spacing 44 which forms a trench 45, performing chemical mechanical planarization to remove portions of layer 60. After planarization of layer 60, a top surface 66 of layer 60 in spacing 44 and a top surface 68 of layer 60 in spacing 46 are etched by an oxide etch selective to nitride. After layer 60 is subjected to an oxide etch, structure 12 is subjected to thermal oxidation to grow the oxide in spacings 44 and 46 by local oxidation of silicon (LOCOS) techniques. This patent discloses that the further growing of layers 60 in spacings 44 and 46, by the thermal oxidation, provides a deeper insulative region in both regions 24 and 28 of structure 12; and that once subjected to thermal oxidation, the insulative material in regions 24 and 28 grows in a direction towards nitride layer 18 and base 14.

It is emphasized that according to the technique described in Mehta, et al., after planarization of layer 60 a top surface 66 of layer 60 in spacing 44 and a top surface 68 of layer 60 in spacing 46 are etched by an oxide etch selective to nitride. It is respectfully submitted that this teaching in Mehta, et al. would have neither disclosed nor would have suggested, and in fact would have taught away from, the subject matter according to the present invention, including wherein the polished surface formed by the chemical mechanical polishing is subjected to thermal oxidation. In other words, it is emphasized that according to the present invention the additional thermal oxidation is performed on the structure having the polished surface; in contrast, in Mehta, et al. an additional etching step is performed after planarization and prior to thermal oxidation, such that it is not the planarized structure (structure with the chemically mechanically polished surface) which is

subjected to the thermal oxidation.

In addition, it is emphasized that according to Mehta, et al. the additional thermal oxidation is performed to provide a deeper insulative region in both regions 24 and 28 of structure 12; that is, when subjected to thermal oxidation, the insulative material in regions 24 and 28 grows in a direction towards nitride layer 18 and towards base 14. See column 5, lines 55-61 of Mehta, et al. It is respectfully submitted that this disclosure would have neither taught nor would have suggested, and in fact would have taught away from, the presently claimed invention, including the selective thermal oxidation at the upper end portion of the trench, and advantages thereof as achieved according to the present invention.

It is emphasized that according to the present invention, the upper portion of the trench is selectively oxidized, with the buried insulating film being used so as not to substantially oxidize the bottom of the trench. Since the upper portion of the trench is selectively oxidized to obtain larger curvature at the upper corners, advantages according to the present invention are achieved. In contrast, Mehta, et al. performs the additional oxidation for a different purpose, to grow the oxide in a direction towards, inter alia, the base. Accordingly, Mehta, et al. would have neither taught nor would have suggested the present invention, and advantages thereof.

It is emphasized that Mehta, et al. requires an etching back of the burying material in, e.g., the trench, prior to the thermal oxidation, so as to thin the insulating material in the trench, whereby an oxidizing seed can easily reach the bottom of the trench so that, in the oxidation after reducing the insulating film thickness buried in

the trench, the oxide grows in a direction toward the base. This is opposite to the present invention, which utilizes selective oxidation at the upper portion of the trench. Clearly, the teachings of Mehta, et al. would not have disclosed nor would have suggested the presently claimed invention, including advantages thereof.

It is respectfully submitted that the additional teachings of Kojiro would not have rectified the deficiencies of Mehta, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Kojiro discloses a technique for forming a semiconductor device in which an oxide film is easily buried and a trench for applying a small leakage current is formed when it is used as an isolation of elements, by forming a taper in the opening of the trench. In particular, this patent discloses that, with an oxide film 2 as a mask, a silicon substrate 1 is isotropically plasma-etched, to provide a recess of circular-arc-shaped section. Further, the recess is anisotropically etched with the film 2 as a mask, so as to form a trench 3 of desired depth, the film 2 of the mask then being removed. The formed trench has a taper 3a in the opening; and, thereafter, when burying the trench with an oxide film and a flattening technique by an etching-back method are applied, the isolation of elements due to the trench buried with the film 4 is completed.

Even assuming, arguendo, that the teachings of Kojiro were properly combinable with the teachings of Mehta, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed method, including, inter alia, wherein the structure with the tapered trench is subjected to the additional oxidation, providing advantages as discussed previously, particularly

where such additional oxidation is performed after removing the insulating film on the oxidation prevention film, especially where the structure having the chemically-mechanically polished surface is subjected to the additional oxidation.

Mehta '599 discloses a combination of (1) trench isolation and (2) local oxidation of silicon, as isolation processes. See column 1, lines 8-10. The process described in Mehta includes forming a first insulation region and a second insulation region, etching a trench in the first insulation region, the trench extending into the semiconductor substrate to a depth below the surface of the semiconductor substrate; filling the first insulation region with an isolation material and removing a portion of the isolation material such that the trench isolation material fills the trench and has a surface level with the surface of a substrate; and thermally growing a field oxide in the first and second insulation region. Note the paragraph bridging columns 3 and 4 of this patent. See also column 4, lines 47-51; column 5, lines 37-42 and 64-67; and column 6, lines 4-9 and 19-23.

As with Mehta, et al., Mehta '599 describes an additional etching to the level of the silicon substrate, after chemical mechanical polishing. See column 6, lines 15-17, of Mehta '599, describing an etching step performed after the, e.g., chemical mechanical polishing described in column 6, lines 4-14. After this further etching, the field oxidation step is performed. As with Mehta, et al., it is respectfully submitted that Mehta '599 would have neither taught nor would have suggested, and in fact would have taught away from, the presently claimed process, including wherein the structure having the polished surface is thermally oxidized by the additional thermal oxidation, achieving advantages of the present invention as

discussed previously.

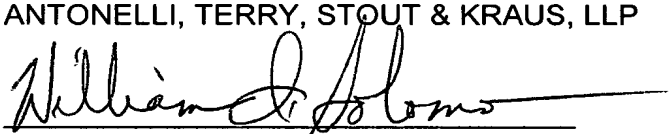
In view of the foregoing comments and amendments, reconsideration and allowance of all claims remaining in the application are respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The changes are shown on the attachment captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (500.36904X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Five Times Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of said semiconductor substrate, said trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in said semiconductor substrate, exposed in said trench;

(d) burying a buried insulating film into said trench so oxidized, said insulating film also being formed on the oxidation prevention film;

(e) after burying said buried insulating film, removing said insulating film on the oxidation prevention film, by chemical mechanical polishing, thereby forming a polished surface;

(f) after said removing, [oxidizing] performing oxidation of said semiconductor substrate having said polished surface, so as to oxidize only a portion of said semiconductor substrate, at said upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench, so as to provide a curvature of the upper end portion of the trench;

(g) eliminating said oxidation prevention film formed on said semiconductor substrate; and

(h) after said eliminating, forming a gate oxide film.

2. (Five Times Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming shallow trenches having a radius of curvature at corners in a desired position of the circuit formation surface of said semiconductor substrate;

(c) forming trenches having a predetermined depth to said shallow trenches having a radius of curvature so formed;

(d) oxidizing trench portions formed in said semiconductor substrate, exposed in said trenches;

(e) burying a buried insulating film into said trenches so oxidized, with said insulating film being formed on said oxidation prevention film;

(f) removing said insulating film formed on said oxidation prevention film, by chemical mechanical polishing, thereby forming a polished surface;

(g) [oxidizing] after said removing, performing oxidation of said semiconductor substrate having said polished surface, so as to oxidize only a portion of the semiconductor substrate extending from said corners, and not substantially at other portions of the semiconductor substrate lining the trenches, [after said removing,] so as to increase the radius of curvature of the shallow trenches;

(h) eliminating said oxidation prevention film formed on said

semiconductor substrate; and

(i) after said eliminating, forming a gate oxide film.

4. (Five Times Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming trenches having a predetermined depth at desired positions of the circuit formation surface of said semiconductor substrate, said trenches having upper end portions not covered by said oxidation prevention film;

(c) oxidizing trench portions formed in said semiconductor substrate, exposed in said trenches;

(d) burying a buried insulating film into said trenches so oxidized, said insulating film also being formed on said oxidation prevention film;

(e) removing said insulating film on said oxidation prevention film, by chemical mechanical polishing, thereby forming a polished surface;

(f) after said removing, [oxidizing] performing oxidation of said semiconductor substrate having said polished surface, so as to oxidize only a portion of said semiconductor substrate at said upper end portions of said trenches, and not substantially at other portions of the semiconductor substrate lining the trenches, said upper end portions not covered by said oxidation prevention film being oxidized;

(g) removing said oxidation prevention film formed on the circuit formation

surface of said semiconductor substrate; and

(h) after said oxidizing said semiconductor substrate, forming a gate oxide film.

5. (Five Times Amended) A method of fabricating a semiconductor substrate comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming shallow trenches having a radius of curvature at corners in desired positions of the circuit formation surface of said semiconductor substrate;

(c) forming trenches having a predetermined depth in said shallow trenches having a radius of curvature;

(d) oxidizing trench portions formed in said semiconductor substrate, exposed in said trenches;

(e) burying a buried insulating film into said trenches so oxidized, said insulating film also being formed on said oxidation prevention film;

(f) removing said insulating film formed on said oxidation prevention film, by chemical mechanical polishing, thereby forming a polished surface;

(g) after said removing, [oxidizing] performing oxidation of said semiconductor substrate having said polished surface, so as to oxidize only a portion of said semiconductor substrate extending from said corners, and not substantially at other portions of the semiconductor substrate lining the trenches, so as to increase the radius of curvature of the shallow trenches at said corners;

(h) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate; and

(i) after said oxidizing said semiconductor substrate, forming a gate oxide film.

9. (Five Times Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate,

(b) forming trench regions in said substrate from said circuit formation surface thereof,

(c) performing a first oxidation to form an oxide film on said trench regions formed in step (b), and

(d) forming an insulating film inside said oxidized trench regions so as to completely fill them, thereby forming completely filled trench regions, and forming the insulating film on the oxidation prevention film,

characterized by further steps of:

(e) removing said insulating film formed on the oxidation prevention film, ~~by chemical mechanical polishing, thereby forming a polished surface;~~

(f) after said removing, performing a second oxidation, of said semiconductor substrate having said polished surface, so as to selectively oxidize only an opening side of said completely filled trench regions in said substrate; and

(g) after performing the second oxidation, removing said oxidation

prevention film, and forming a gate oxide film.

10. (Four Times Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of said semiconductor substrate, the trench having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in said semiconductor substrate, exposed in said trench;

(d) burying a buried insulating film into said trench so oxidized, the insulating film also being formed on the oxidation prevention film;

(e) removing the insulating film formed on the oxidation prevention film by chemical mechanical polishing, thereby forming a polished surface;

(f) after said removing, [oxidizing] performing oxidation of said semiconductor substrate having said polished surface, so as to oxidize only a portion of the semiconductor substrate, at the upper end portion of said trench and not substantially at other portions of the semiconductor substrate lining the trench, to provide the upper end portion with a curvature;

and

(g) removing said oxidation prevention film formed on the circuit formation

surface of said semiconductor substrate.

15. (Four Times Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of said semiconductor substrate, the trench having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in said semiconductor substrate, exposed in said trench, so as to provide the upper end portion of said trench with a curvature;

(d) burying a buried insulating film into said trench so oxidized, the insulating film also being formed on the oxidation prevention film;

(e) removing said insulating film formed on said oxidation prevention film, having said buried insulating film in said trench, by chemical mechanical polishing, thereby forming a polished surface;

(f) after said removing, performing thermal oxidation of [the] said semiconductor substrate having said polished surface only at the upper end portion of the trench, to increase the curvature of the upper end portion of the trench as compared with the curvature provided in step (c); and

(g) removing said oxidation prevention film formed on the circuit formation

surface of said circuit substrate.

41. (Twice Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of said semiconductor substrate, said trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in said semiconductor substrate, exposed in said trench, forming a curvature of said upper end portion of said trench;

(d) burying a buried insulating film into said trench so oxidized, the insulating film also being formed on the oxidation prevention film;

(e) removing the insulating film formed on the oxidation prevention film, by chemical mechanical polishing, thereby forming a polished surface;

(f) after said removing, [selectively oxidizing] performing selective oxidation of said semiconductor substrate having said polished surface, at said upper end portion so as to provide an increased curvature of the upper end portion of the trench as compared with the curvature formed in step (c);

(g) eliminating said oxidation prevention film formed on said semiconductor substrate; and

(h) after said eliminating, forming a gate oxide film.

43. (Twice Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming shallow trenches having a radius of curvature at corners in a desired position of the circuit formation surface of said semiconductor substrate;

(c) forming trenches having a predetermined depth to said shallow trenches having a radius of curvature so formed;

(d) oxidizing trench portions formed in said semiconductor substrate, exposed in said trenches;

(e) burying a buried insulating film into said trenches so oxidized, said insulating film also being formed on the oxidation prevention film;

(f) removing said insulating film formed on the oxidation prevention film, by chemical mechanical polishing, thereby forming a polished surface;

(g) [selectively oxidizing] performing the selective oxidation of the semiconductor substrate having said polished surface, after said removing, so as to increase the radius of curvature at the corners of the shallow trenches as compared to the radius of curvature formed in step (b);

(h) eliminating said oxidation prevention film formed on said semiconductor substrate; and

(i) after said eliminating, forming a gate oxide film.

45. (Twice Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming trenches having a predetermined depth at desired positions of the circuit formation surface of said semiconductor substrate, said trenches having upper end portions not covered by said oxidation prevention film;

(c) oxidizing trench portions formed in said semiconductor substrate, exposed in said trenches, so as to provide a curvature at said upper end portions of the trenches;

(d) burying a buried insulating film into said trenches so oxidized, the insulating film also being formed on the oxidation prevention film;

(e) removing the insulating film on the oxidation prevention film, by chemical mechanical polishing, thereby forming a polished surface;

(f) [selectively oxidizing] performing selective oxidation of said semiconductor substrate having said polished surface after said insulating film formed on said oxidation prevention film is removed, said upper end portions not covered by said oxidation prevention film being oxidized;

~~(g) removing said oxidation prevention film formed on the circuit formation~~ surface of said semiconductor substrate; and

(h) after said oxidizing said semiconductor substrate, forming a gate oxide film.

46. (Twice Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate,

(b) forming trench regions in said substrate from said circuit formation surface thereof,

(c) performing a first oxidation to form an oxide film on said trench regions formed in step (b), so as to provide a curvature at an opening side of the trench regions, and

(d) forming an insulating film inside said oxidized trench regions so as to completely fill them, the insulating film also being formed on the oxidation prevention film

characterized by further steps of:

(e) removing said insulating film formed on the oxidation prevention film, by chemical mechanical polishing, thereby forming a polished surface;

(f) after said removing, performing a selective second oxidation of said semiconductor substrate having said polished surface, to selectively oxidize the opening side of said completely filled trench regions in said substrate, so as to provide an increased curvature at the opening side as compared to said curvature provided in step (c); and

(g) after performing the second oxidation, removing said oxidation prevention film and forming a gate oxide film.

47. (Amended) A method of fabricating a semiconductor device comprising the steps of:

a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of said semiconductor substrate, the trench having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in said semiconductor substrate, exposed in said trench, thereby providing the upper end portion of the trench with a radius of curvature;

(d) burying a buried insulating film into said trench so oxidized, said insulating film also being formed on the oxidation prevention film;

(e) removing said insulating film formed on the oxidation prevention film, by chemical mechanical polishing, thereby forming a polished surface;

(f) after said removing, providing the upper end portion of said trench with an increased radius of curvature, as compared with the radius of curvature provided in step (c), by [selectively oxidizing] performing selective oxidation of the upper end portion of the trench of said semiconductor substrate having the polished surface;

and

(g) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate.